

1. Description

The 50N06DA is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD inverter, computer power management and DC to DC converter circuits which need low in-line power loss.

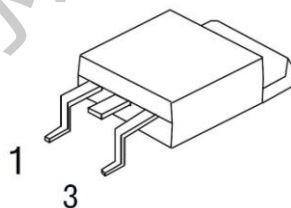
2. Feature

- $R_{DS(ON)} \leq 22m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

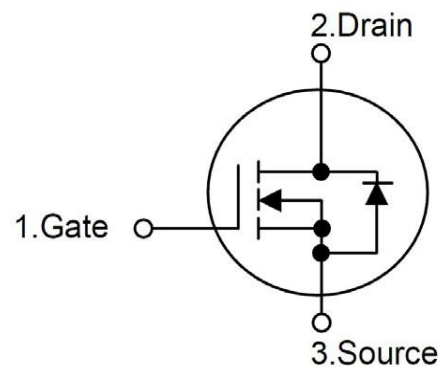
V_{DS}	60	V
$R_{DS(on)}$	22	m Ω
I_D	50	A

3. Pin configuration

Order Number	Package
50N06DA	TO-252



TO-252



4. Absolute maximum ratings (Tc=25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate-Source Voltage		V _{DSS}	±20	V
Continuous Drain Current	Tc=25°C	I _D	50	A
	Tc=70°C		35.1	A
Pulsed Drain Current		I _{DM}	140	A
Power Dissipation	Tc=25°C	P _D	60	W
	Tc=70°C		38.5	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 175	°C

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case to sink typ.	R _{thCS}	0.5	°C/W
Thermal resistance junction to case.	R _{thJC}	2.1	°C/W
Thermal resistance junction to ambient.	R _{thJA}	110	°C/W

6. Electrical characteristics (TA =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250μA	60	–	–	V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA	2	–	4	V
IGSS	Gate-Body Leakage	VDS=0V, VGS=±20V	–	–	±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=60V, VGS=0V	–	–	1	μA
RDS(ON)	Drain-Source On-Resistance	VGS=10V, ID=50A	–	17	22	mΩ
VSD	Diode Forward Voltage	IS=50A, VGS=0V	–	1	1.2	V
DYNAMIC						
Qg	Total Gate Charge	VDD=48V, VGS=10V, ID=50A	–	37	–	Nc
Qg	Total Gate Charge	VDD=48V, VGS=4.5V, ID=50A	–	11	–	
Qgs	Gate-Source Charge		–	15	–	
Qgd	Gate-Drain Charge		–	8	–	
Rg	Gate Resistance	VDS=0V, VGS=0V, f=1MHz	–	2	–	Ω
Ciss	Input Capacitance	VDS=15V, VGS=0V, f=1MHz	–	2270	–	pF
Coss	Output Capacitance		–	197	–	
Crss	Reverse Transfer Capacitance		–	62	–	
td(on)	Turn-On Delay Time	VGS =10V, RL=30Ω VDS=30V, RG=3.6Ω	–	29	–	ns
tr	Turn-On Rise Time		–	5	–	
td(off)	Turn-Off Delay Time		–	53	–	
tf	Turn-Off Fall Time		–	6	–	

Notes :

pulse test:pulse width ≤ 300 us,duty cycle 2% ,Guaranteed by design,not subject to production testing.

