

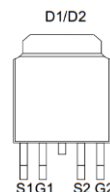
Features

- N Channel: 30V, 20A / P Channel: -30V, -20A
- N: $R_{DS(ON)} = 13m\Omega$ (Max.) @ $V_{GS} = 10V$, $I_D = 10A$
- P: $R_{DS(ON)} = 26m\Omega$ (Max.) @ $V_{GS} = -10V$, $I_D = -10A$
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{as}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

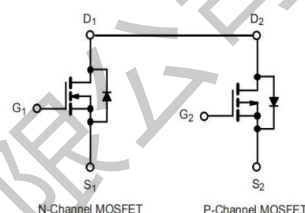
- H-bridge
- Inverters

Package



TO-252-4L

SFDA45Y03AT



Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise specified

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		± 20	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	20	-20	A
		$T_C = 100^\circ C$	20	-17.9	A
I_{DM}	Pulsed Drain Current ^{note1}		40	-40	A
P_D	Power Dissipation	$T_C = 25^\circ C$	31		W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		4		$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175		$^\circ C$

*Drain current limited by maximum junction temperature

N-Channel Electrical Characteristics $T_C=25^{\circ}\text{C}$ unless otherwise specified

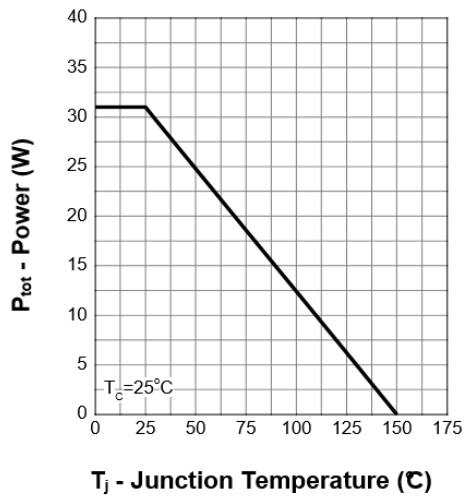
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24V, V _{GS} = 0V	-	-	1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.0	-	2.0	V
R _{DS(on)}	Static Drain-Source On-Resistance ^{note2}	V _{GS} = 10V, I _D = 10A	-	10.5	13	mΩ
		V _{GS} = 4.5V, I _D = 5A	-	13.5	17	
g _{FS}	Forward Transconductance	V _{DS} = 10V, I _D = 7A	-	29	-	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1.0MHz	-	1181	-	pF
C _{oss}	Output Capacitance		-	107	-	pF
C _{rss}	Reverse Transfer Capacitance		-	90	-	pF
Q _g	Total Gate Charge	V _{DS} = 15V, I _D = 10A, V _{GS} = 10V	-	22	-	nC
Q _{gs}	Gate-Source Charge		-	5	-	nC
Q _{gd}	Gate-Drain Charge		-	3.3	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DS} = 15V, R _L = 1.5Ω R _G = 4.5Ω, V _{GEN} = 10V	-	7	-	ns
t _r	Turn-On Rise Time		-	30	-	ns
t _{d(off)}	Turn-Off Delay Time		-	19	-	ns
t _f	Turn-Off Fall Time		-	18	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S =10A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 10A,	-	34	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt =100A/μs	-	7.1	-	nC

Notes:

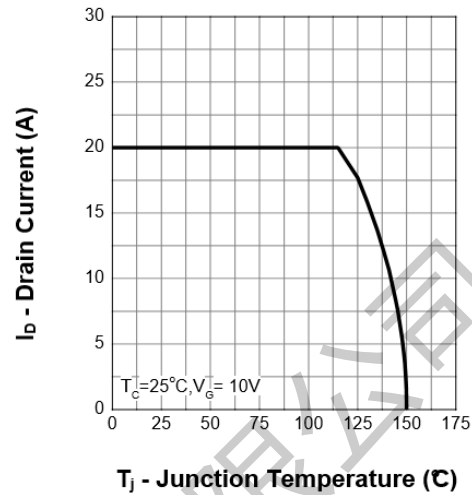
- 1.Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- 2.Surface Mounted on FR4 Board, $t_s \leq 10\text{sec}$

N-Channel Typical Performance Characteristics

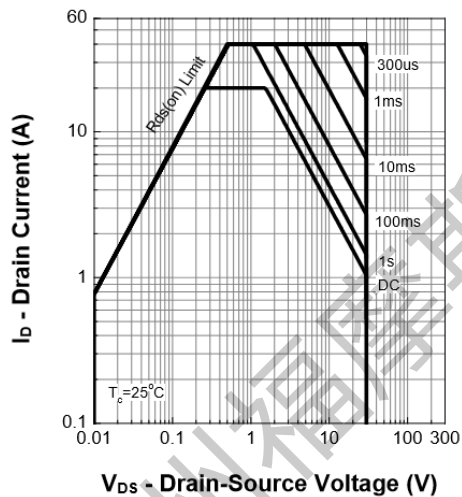
Power Capability



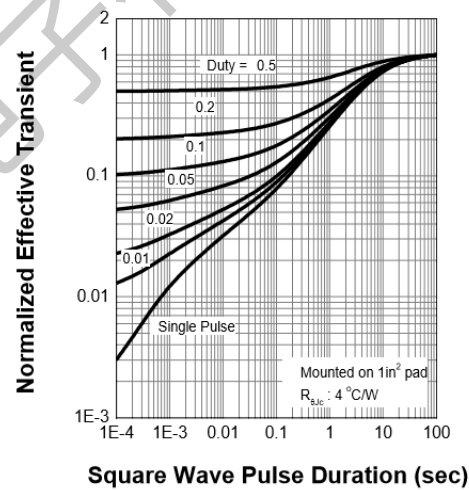
Current Capability



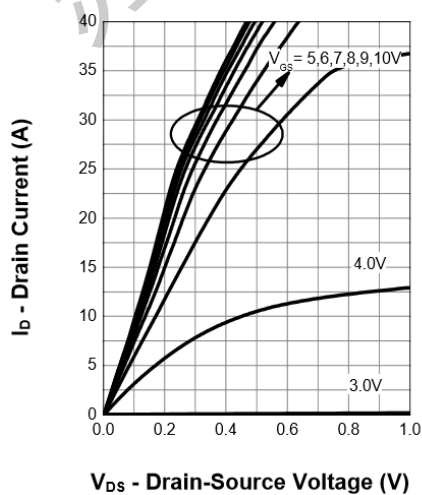
Safe Operation Area



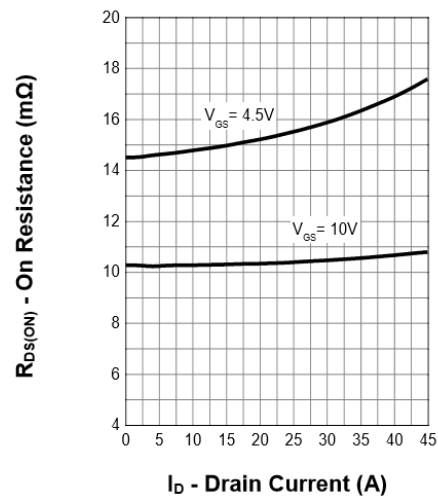
Thermal Transient Impedance



Output Characteristics



On Resistance





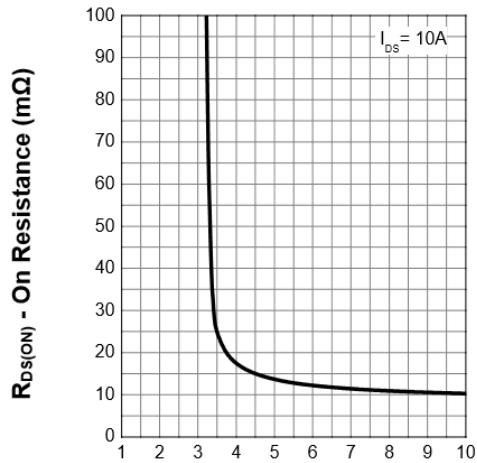
福摩斯
FU MO SI

Silicon N&P-Channel Mosfet

SFDA45Y03AT

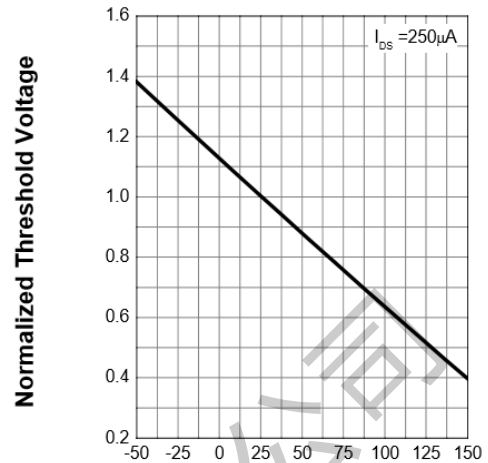


Transfer Characteristics



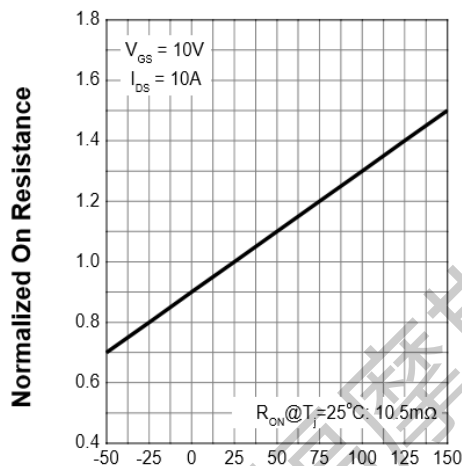
V_{GS} - Gate-Source Voltage (V)

Normalized Threshold Voltage



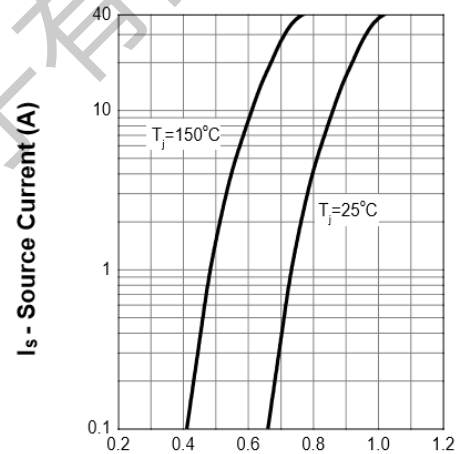
T_J - Junction Temperature (°C)

Normalized On Resistance



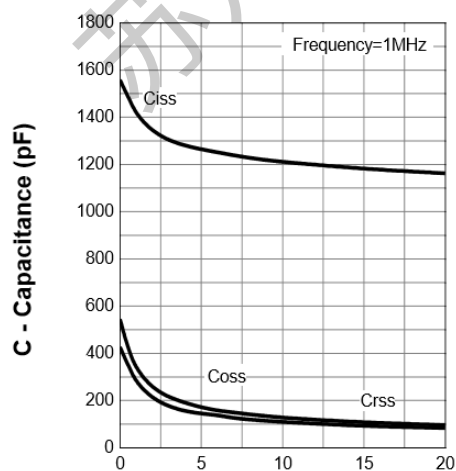
T_J - Junction Temperature (°C)

Diode Forward Current



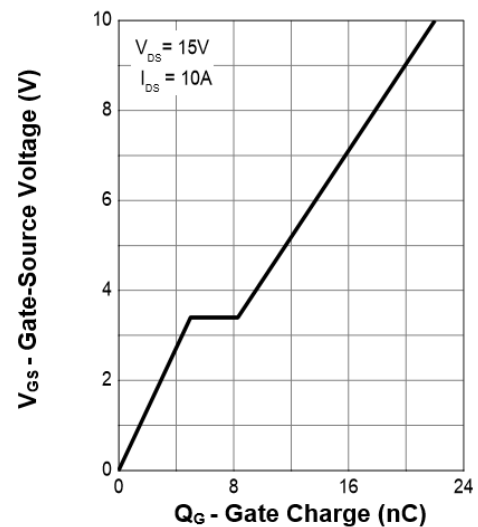
V_{SD} - Source-Drain Voltage (V)

Capacitance



V_{DS} - Drain-Source Voltage (V)

Gate Charge



P-Channel Electrical Characteristics $T_C=25^{\circ}\text{C}$ unless otherwise specified

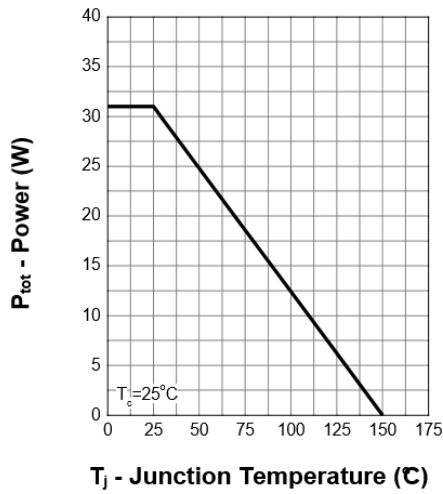
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} = 0V	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-	-2.0	V
R _{DS(on)}	Static Drain-Source On-Resistance ^{note2}	V _{GS} = -10V, I _D = -10A	-	20	26	mΩ
		V _{GS} = -4.5V, I _D = -5A	-	34	44	
g _{FS}	Forward Transconductance	V _{DS} = -5V, I _D = -6A	-	15	-	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1.0MHz	-	1210	-	pF
C _{oss}	Output Capacitance		-	122	-	pF
C _{rss}	Reverse Transfer Capacitance		-	104	-	pF
Q _g	Total Gate Charge	V _{DS} = -15V, I _D = -10A, V _{GS} = -10V	-	22	-	nC
Q _{gs}	Gate-Source Charge		-	5.8	-	nC
Q _{gd}	Gate-Drain Charge		-	3.3	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = -15V, R _L = 1.5Ω R _G = 4.5Ω, V _{GS} = -10V I _{DS} = -10A	-	14	-	ns
t _r	Turn-On Rise Time		-	42	-	ns
t _{d(off)}	Turn-Off Delay Time		-	141	-	ns
t _f	Turn-Off Fall Time		-	75	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-20	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = -10A	-	-	-1.3	V
t _{rr}	Body Diode Reverse Recovery Time	V _{GS} = 0V, I _{SD} = -10A,	-	9.8	-	ns
Q _{rr}	Body Diode Reverse Recovery Time Charge	di/dt = 100A/μs	-	1	-	nC

Notes:

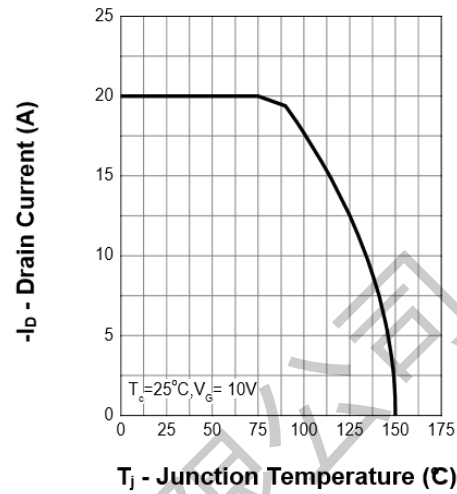
- 1.Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- 2.Surface Mounted on FR4 Board, $t \leq 10\text{sec}$

P-Channel Typical Performance Characteristics

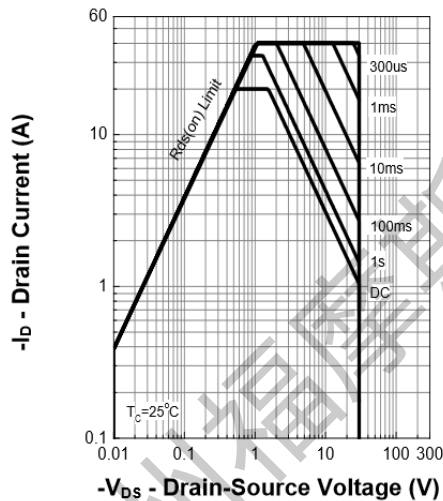
Power Capability



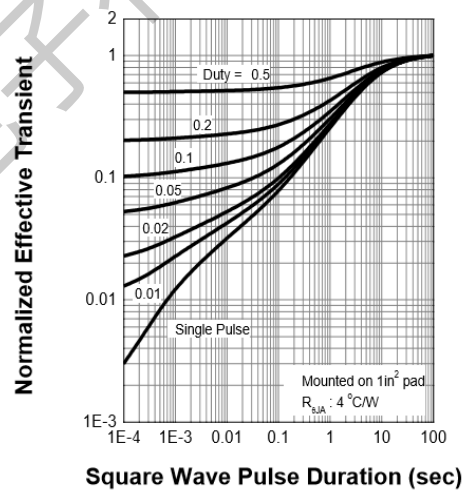
Current Capability



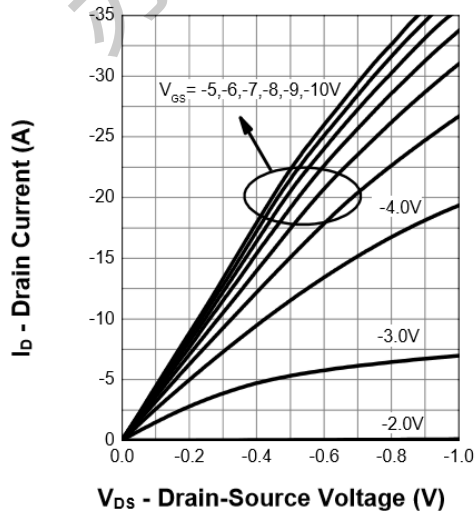
Safe Operation Area



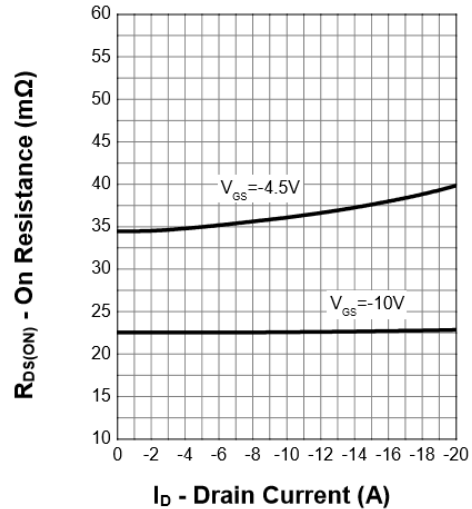
Thermal Transient Impedance



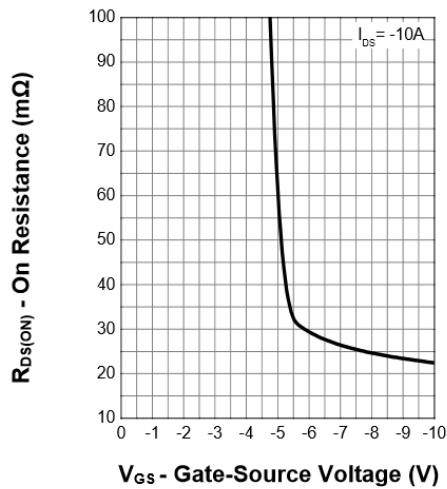
Output Characteristics



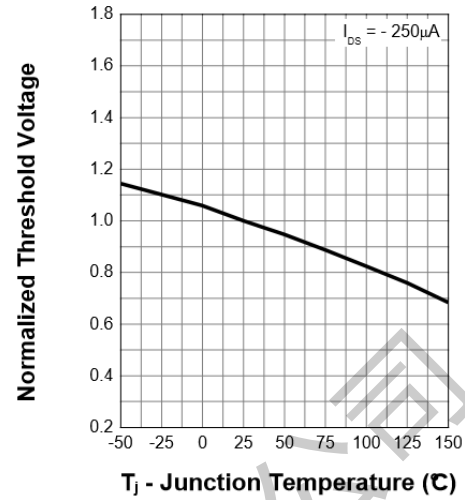
On Resistance



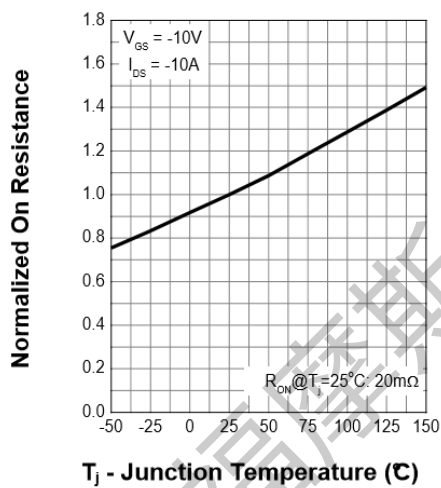
Transfer Characteristics



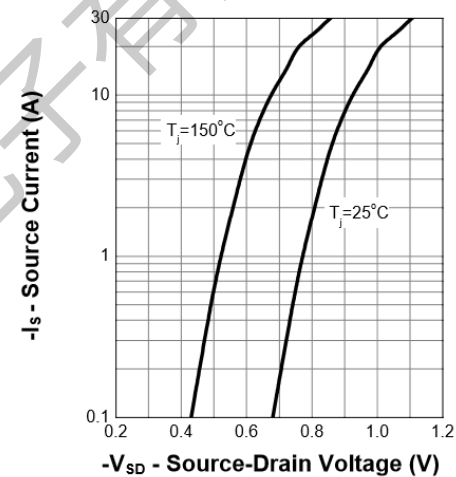
Normalized Threshold Voltage



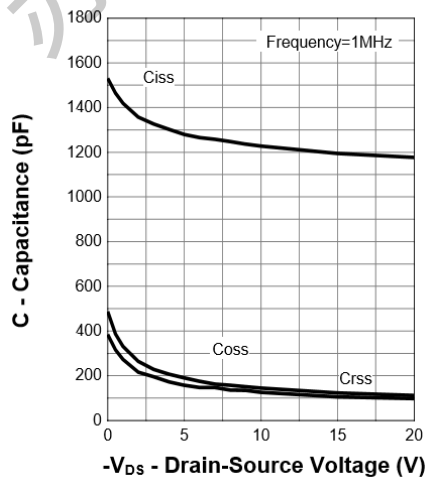
Normalized On Resistance



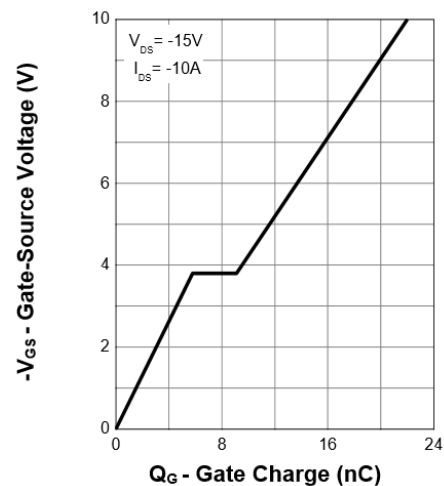
Diode Forward Current



Capacitance



Gate Charge



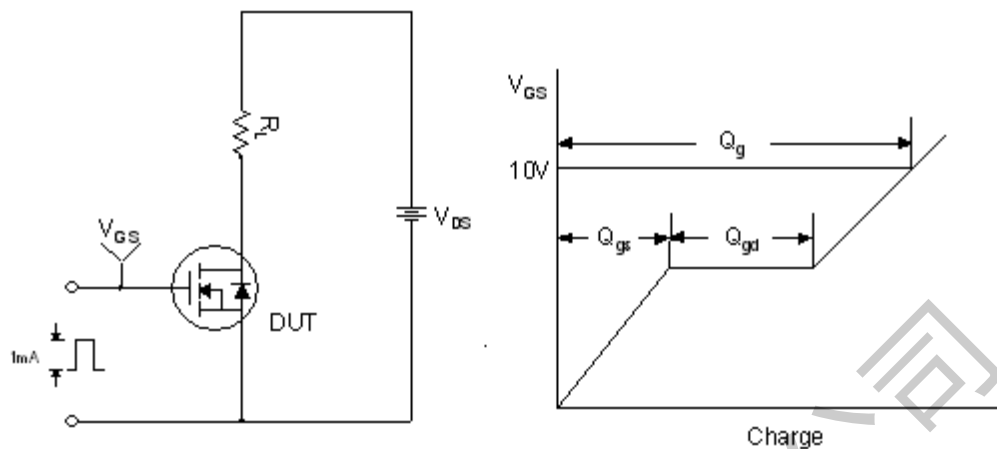


Figure 1. Gate Charge Test Circuit & Waveform

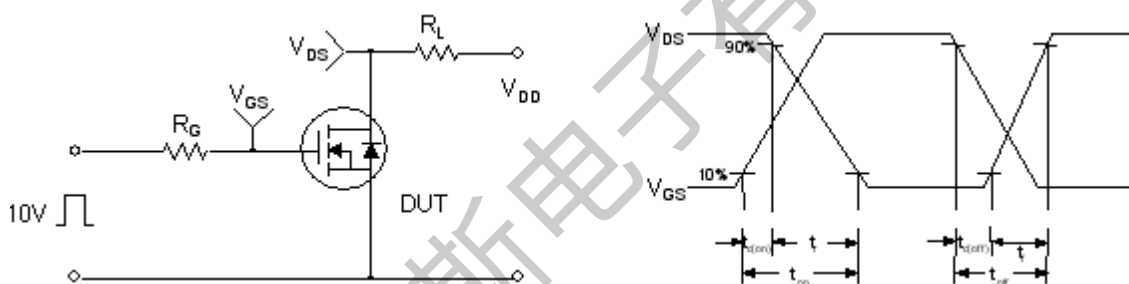


Figure 2. Resistive Switching Test Circuit & Waveforms

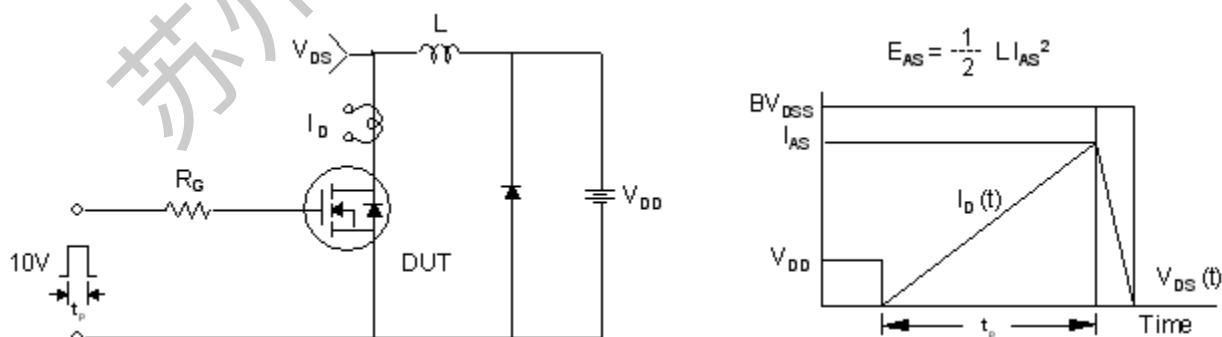
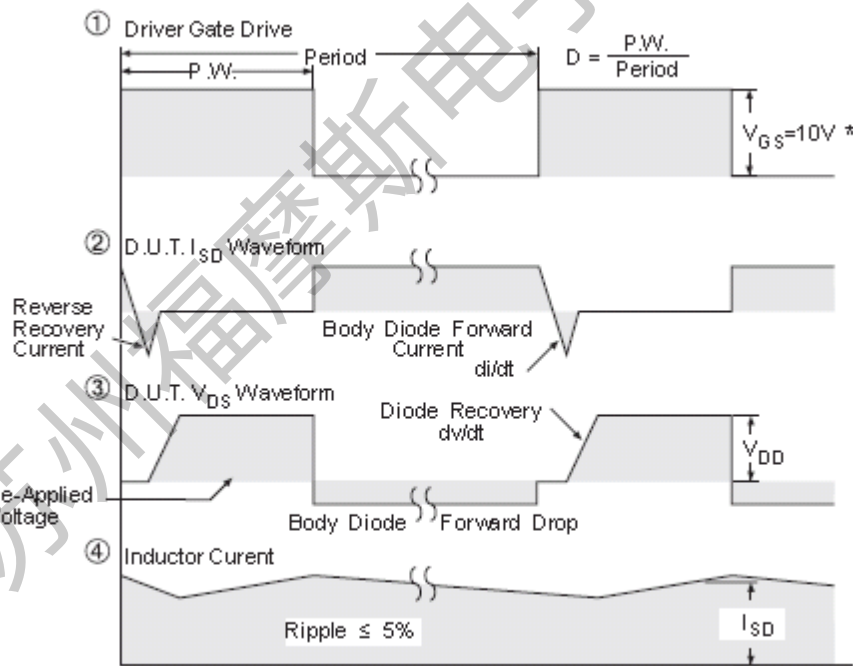
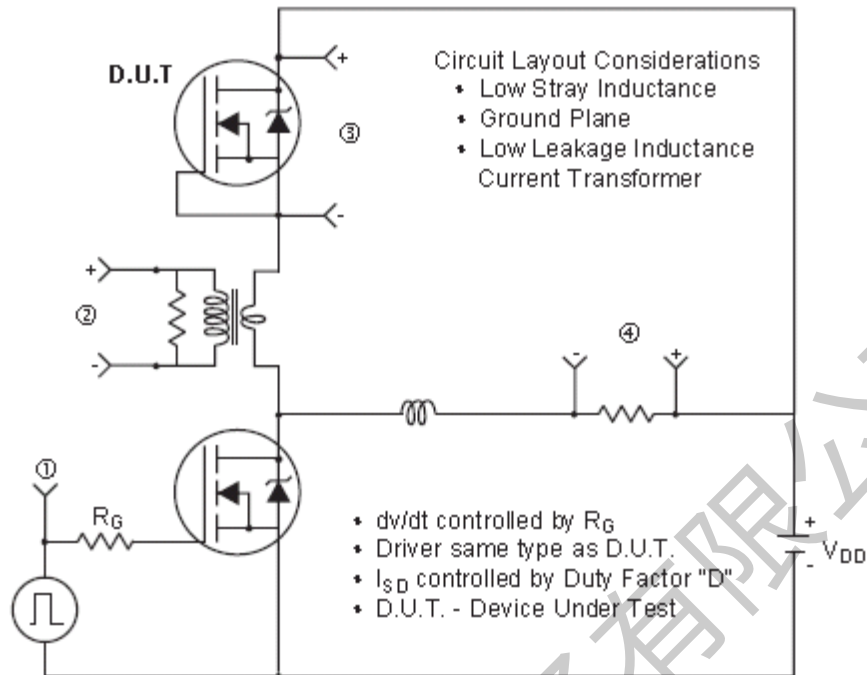


Figure 3. Unclamped Inductive Switching Test Circuit & Waveforms



* $V_{GS} = 5V$ for Logic Level Devices

Figure 4. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)



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